Hes·SO
VALAIS
WALLIS

This is to certify that

Marcelo Kaihara

followed the course "Embedded Systems," which took place between February and May 2019 at the HES-SO Valais-Wallis in Sion, and completed the corresponding labs on digital hardware design. This course covered the topics of FPGA design and synthesis using **VHDL hardware description language**.

Marcelo Kaihara passed the exams and was awarded a

grade B

as defined by the ECTS scale.

Dr. François Corthay
Prof. HES-SO Valais-Wallis